



PTO/SB/08A (08-03)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1 of 3

Complete if Known

Application Number	10/766,786
Filing Date	January 27, 2004
First Named Inventor	Guterman
Art Unit	2827
Examiner Name	M. TRAN
Attorney Docket Number	SAND-01015US0

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
MT		US- 5,220,531	06/15/1993	Blyth et al.	
		US- 5,313,421	05/17/1994	Guterman et al.	
		US- 5,412,601	05/02/1995	Sawada et al.	
		US- 5,521,865	05/28/1996	Ohuchi et al.	
		US- 5,570,315	10/29/1996	Tanaka et al.	
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		US- 5,712,180	01/27/1998	Guterman et al.	
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		US- 6,151,248	11/21/2000	Harari et al.	
		US- 6,222,762	04/24/2001	Guterman et al.	
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		US- 6,301,161	10/09/2001	Holzmann et al.	
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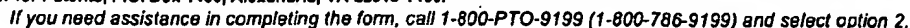
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Examiner Signature	M. TRAN	Date Considered	3/21/05
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Sheet

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of

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
MT		KURATA, Hideaki, et al., Constant-Charge-Injection Programming for 10-MB/s Multilevel AG-AND Flash Memories, 2002 Symposium On VLSI Circuits Digest of Technical Papers, pp. 302-303	
		JOHNSON, William S., et al., SESSION XII: ROMs, PROMs and EROMs, 1980 IEEE International Solid State Circuits Conference, pp. 152-153	
		NOBUKATA, Hiromi, et al., A 144Mb 8-Level NAND Flash Memory with Optimized Pulse Width Programming, 1999 Symposium on VLSI Circuits Digest of Technical Papers, pp. 39-40	
MT		OHKAWA, Masayoshi, et al., TP 2.3: A 98 mm ² 3.3V 64Mb Flash Memory with FN-NOR Type 4-level Cell, 1996 IEEE International Solid-State Circuits Conference, pp. 36-37	

Examiner Signature	M. TRAN	Date Considered	3/22/05
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